iPCB

SMT PCB/Panel layout

PCBA Team

2019-03-22

PCB Design Guideline

Revision record

Rev.	Date	Change Description
0	2019/4/17	New release

Purpose

- Based on the requirements of production process , In the layout and circuit board design process , There is a standard to follow , To achieve high efficiency in the production of assembly , Easy assembly, low cost, and high quality target.
- The content is only applicable to the related database, some are for reference only .

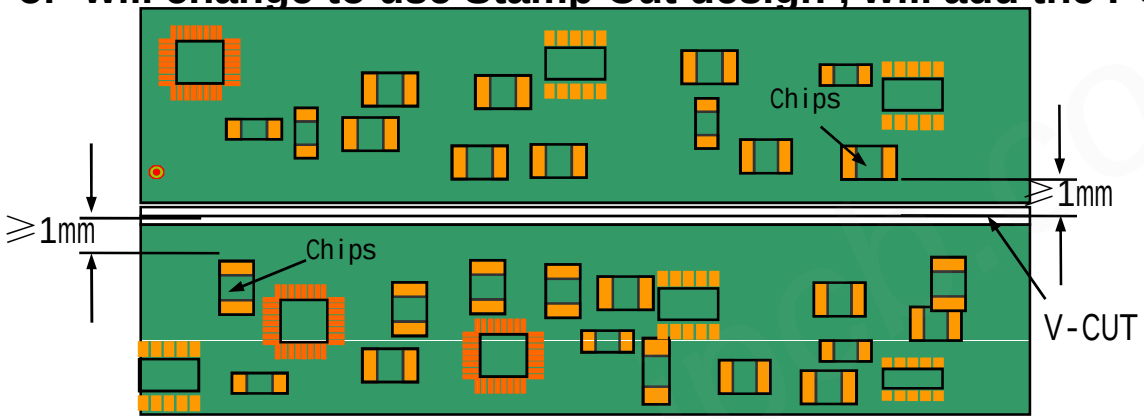
content

- PCB layout rules
- Text marking for silkscreen layer
- PCB Fiducial Mark design
- PCB fixed position hole
- SMT component PAD design
- PTH component PAD design
- Through-hole(Via)design
- Trace design
- other limitation

PCB layout rules

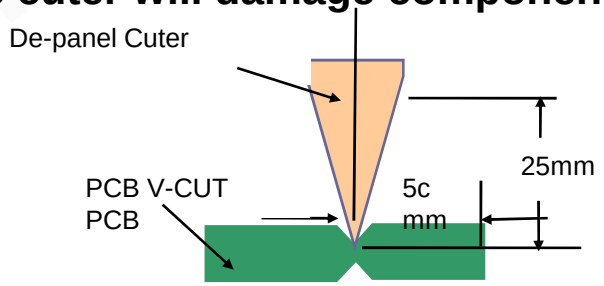
V-Cut layout rule :

- Chips to V-Cut line should be more than 1mm, otherwise will damage chips or will change to use Stamp Cut design , will add the PCB cost



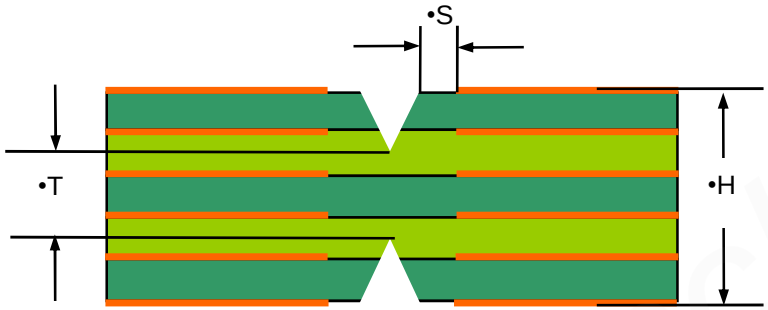
- The distance to PCB edge 0.5mm, can not layout the trace, The distance to PCB edge 1.0mm, can not layout the any component

- The distance to PCB edge 5mm, can not layout the components height over 25mm, otherwise cuter will damage components

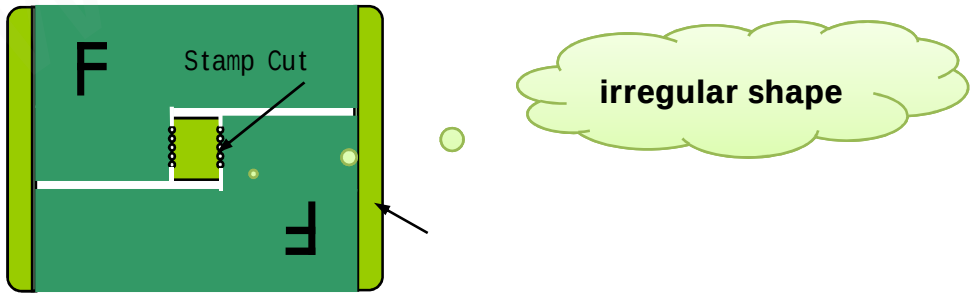


V-Cut layout rules :

- PCB trace to V-Cut should be more then S=0.5mm safety buffer, otherwise will have the risk to damage the trace.



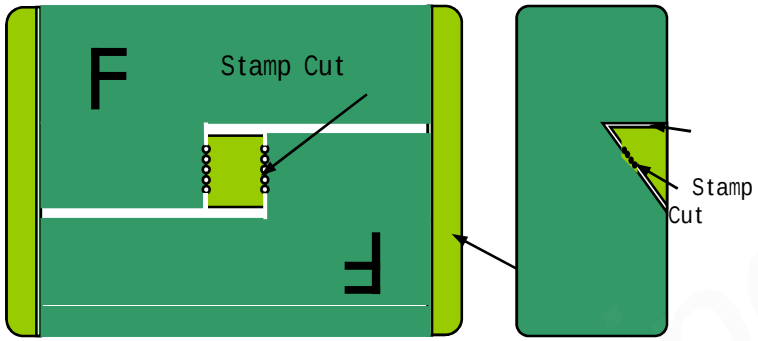
- When we use V-Cut
  - PCB thickness 1.0mm to 3mm(1.0mm to 0.5mm + SMT pallet)
  - PCB outline is square type or rectangle type, irregular shape can not use the V-Cut



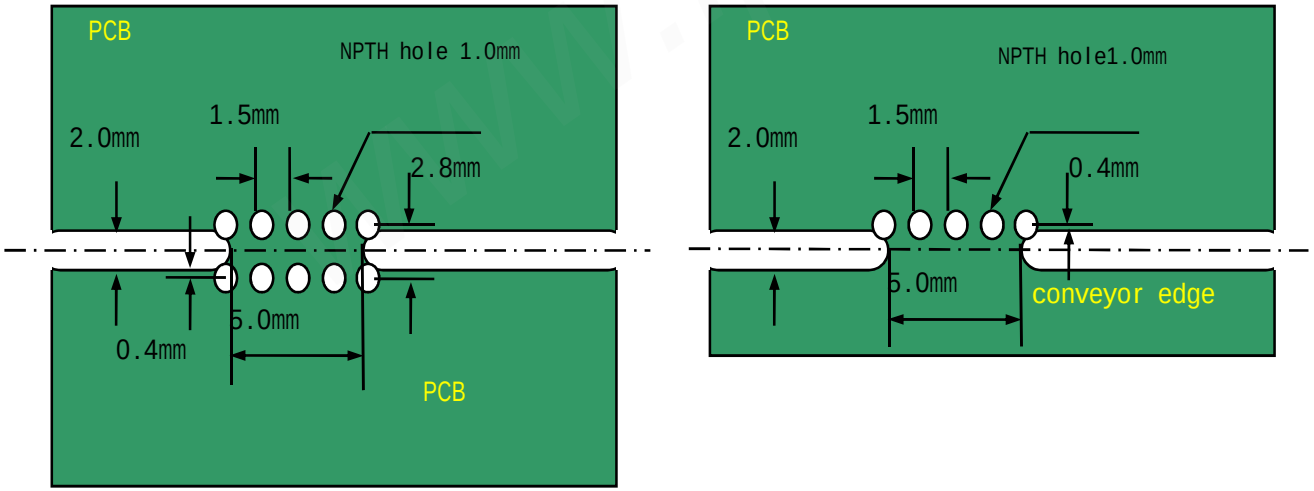
PCB layout rules

Stamp design ：

- Stamp design only for irregular PCB, PCB to PCB layout distance is 2mm, V-Cut only 0.3mm



- Stamp design parameters



PCB layout rules

V-Cut vs Stamp layout :

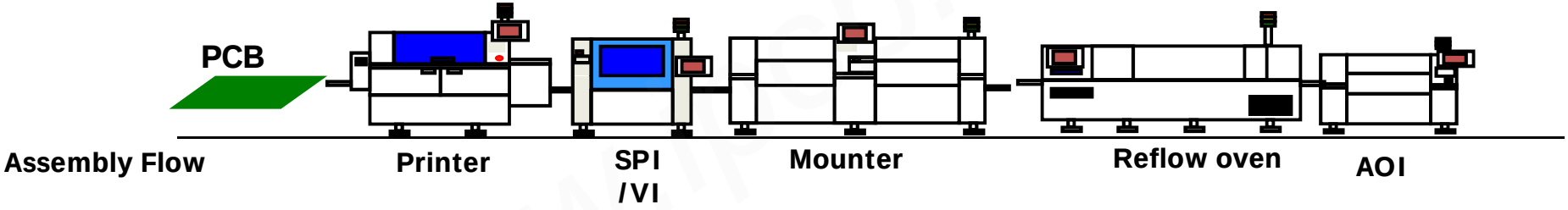
- PCS to PCS distance only 0.3mm for V-Cut, we can save the PCB layout cost
- Stamp Cut design, PCB PCS to PCS distance is 2mm
- Base on same PCS design with different Cut type(stamp/V –Cut), the PCB cost will impact 10- 25%
- V-Cut PCB will be cut by machine, but Stamp Cut will broken by OP and have stress then damage the components

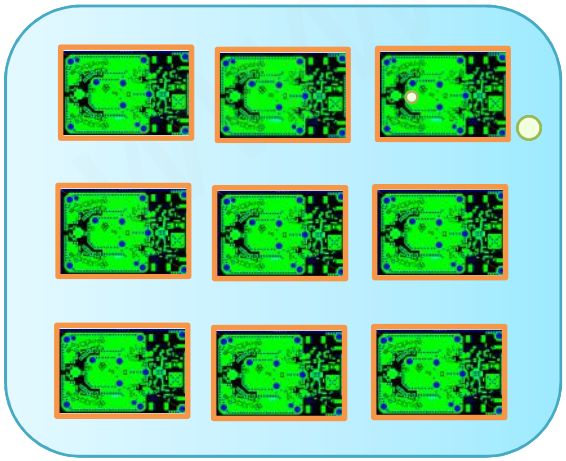
V-Cut machine

PCB / panel layout

Why don’t choose single PCB for SMT process :

- We need to put the each single PCB on carrier when do SMT process
- But carrier cave and single PCB have tolerance , so always happen solder paste printing misalignment then will get the shift/tombstone process issue
- Sometimes will happen single PCB lift up from SMT carrier and will have the chips mounting shift/missing process issues





Put the single PCB on the carrier

PCB / panel layout

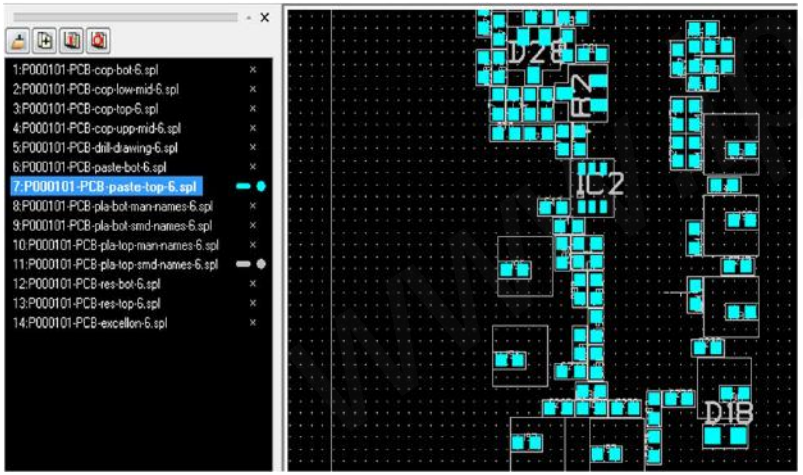
Factors of impact PCB Cost

- PCB layout
  - Fine pitch components
  - Panel V-Cut/Stamp Cut/PCB conveyor edge size
  - PCB drill hole size/quantity
- PCB material cost
- PCB process easy/complicated , process spec
- PCB surface finished process also impact cost, OSP/IMS/EING/IMT
- PCB outline, regular shape is cheaper than irregular shape ,

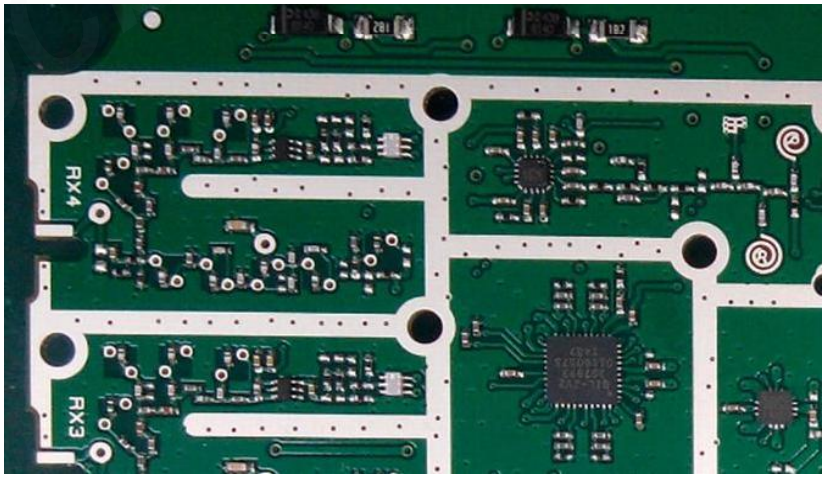
Text marking for silk layer

The current situation:

- We received the gerber file for UK design team ,no silk layer be found
- We can not directly confirm Polarity of component on the PCB , can not confirm the location of component ,easily to confirm IC shift or not .
- In the production adjustment X, Y coordinate and confirmation the location completely rely on engineering drawings ,Big waste of time.

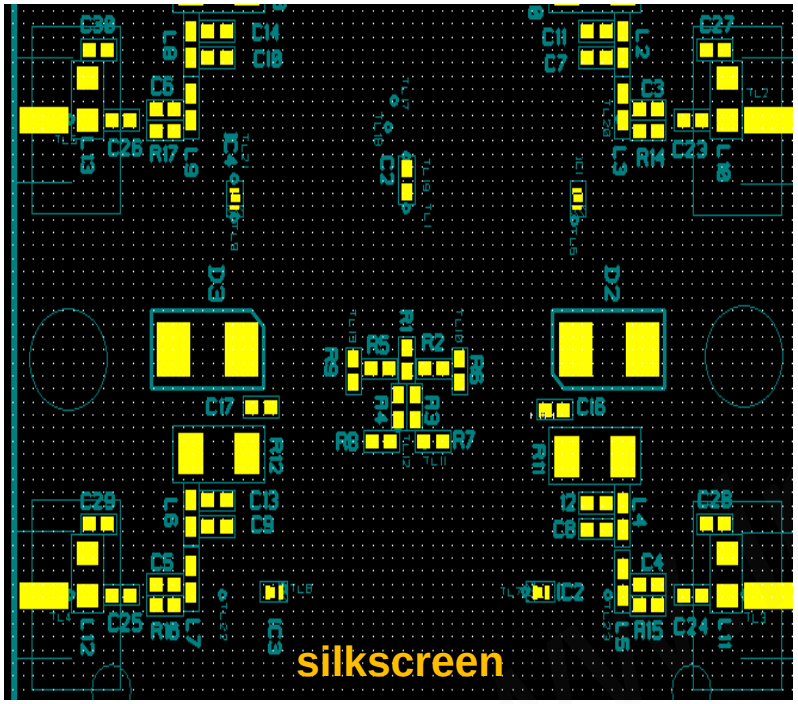


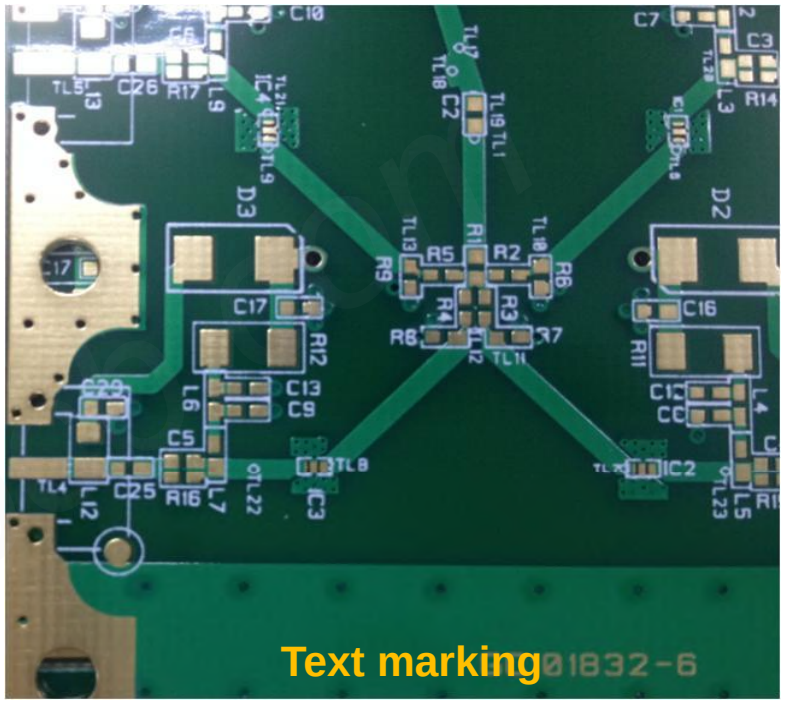
No silk layers in the gerber file



No text mark on the pcb

Text marking for silk layer



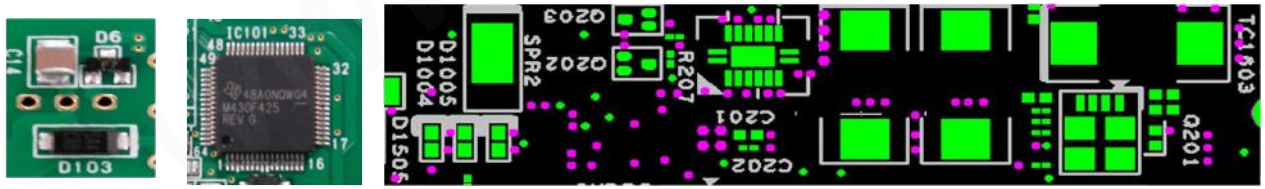


As the icon text marking design we can accept . We can quickly inspection location where there are problems.

Text marking for silk layer

Component outline& polarity marking design definition:

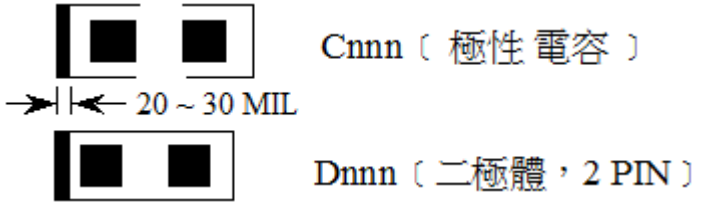
- Text marking, keep away from Via Hole or Through Hole as far as possible
- Text marking , Silk screen printing character, polarity and polarity signs can not components be covered
- Text height≥25 mil ,line width ≥5 mil
- Beside the BGA/CSP ,component outline should not smaller than actual component size.
- The text does not overlap
- SMD/PTH component text marking include body outline , pin assignment ,component name ,polarity marking .as below:



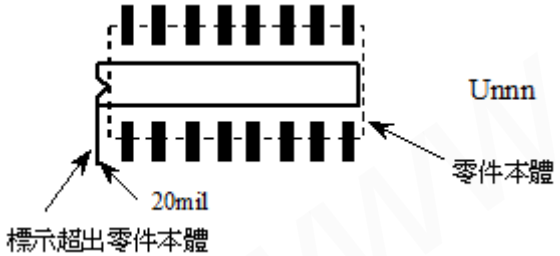
Text marking for silk layer

Component outline& polarity marking

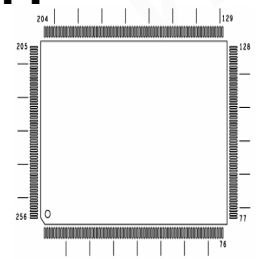
a.Tantalum capacitor or diode（ 3 PIN ）



b.SOP / SSOP



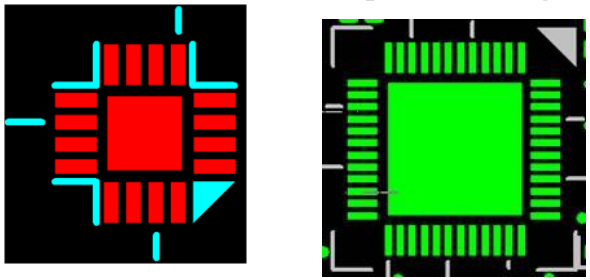
c. QFP



Text marking for silk layer

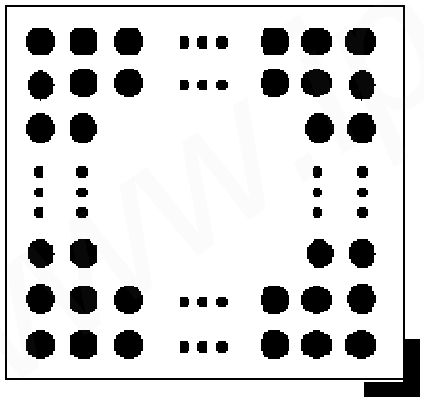
Component outline& polarity marking

d. QFN



e. BGA, CSP marking

-. outline size must the same as actual component



Text marking for silk layer

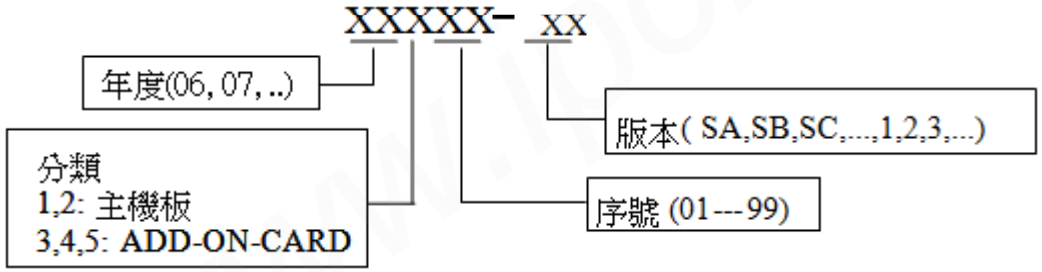
PCB number and version

(i) PCB Model

(ii) PCB Part number and version

(iii) text height : 80mil

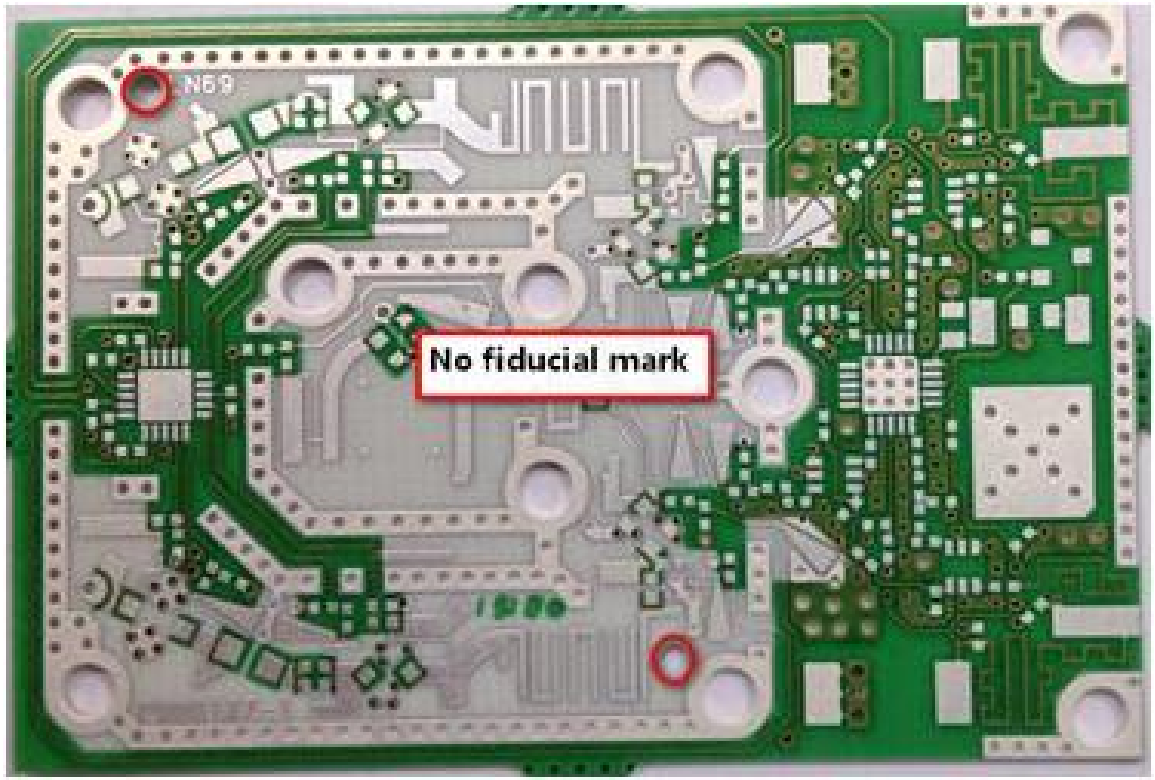
The PCB number is described as follows: the last two codes (06, 07) in AD year



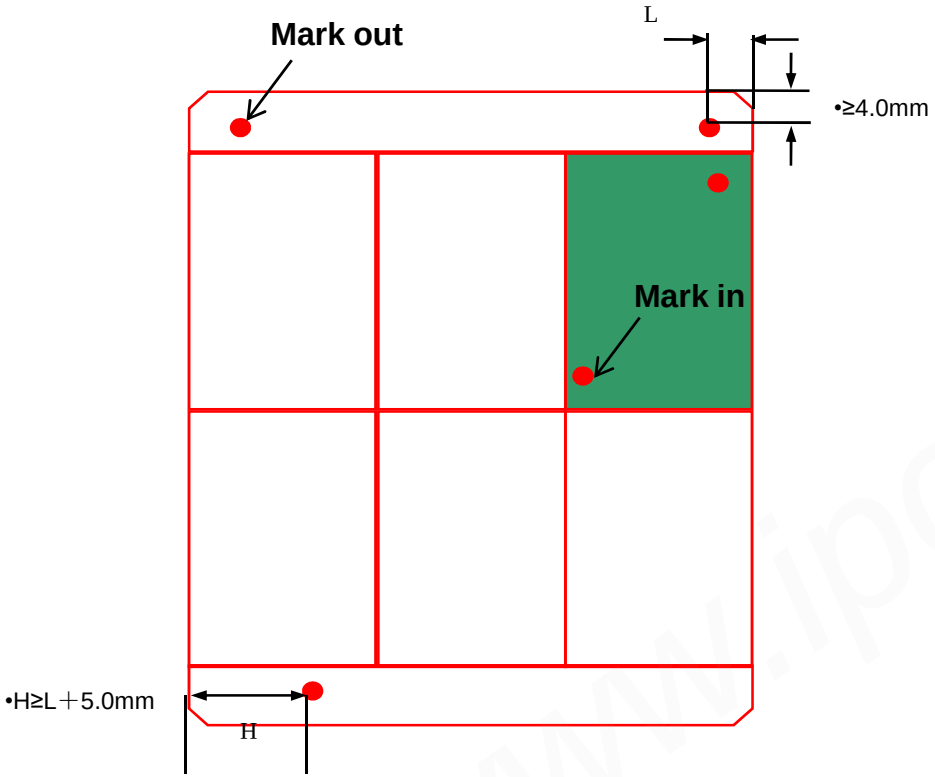
The new PCB must be attached with the board number and - SA (sample a) version. The later modified versions are - SB, - SC, or - 1A, - 1B, - 1C... In order. In mass production, the versions must be - 1, - 2, - 3, etc

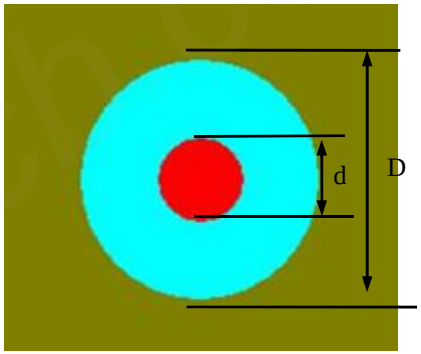
PCB Fiducial Mark design

- **The current situation: Many projects did not design fiducial mark-in, the machine can not recognize to position, cause no high precision print/mounted**



PCB Fiducial Mark design



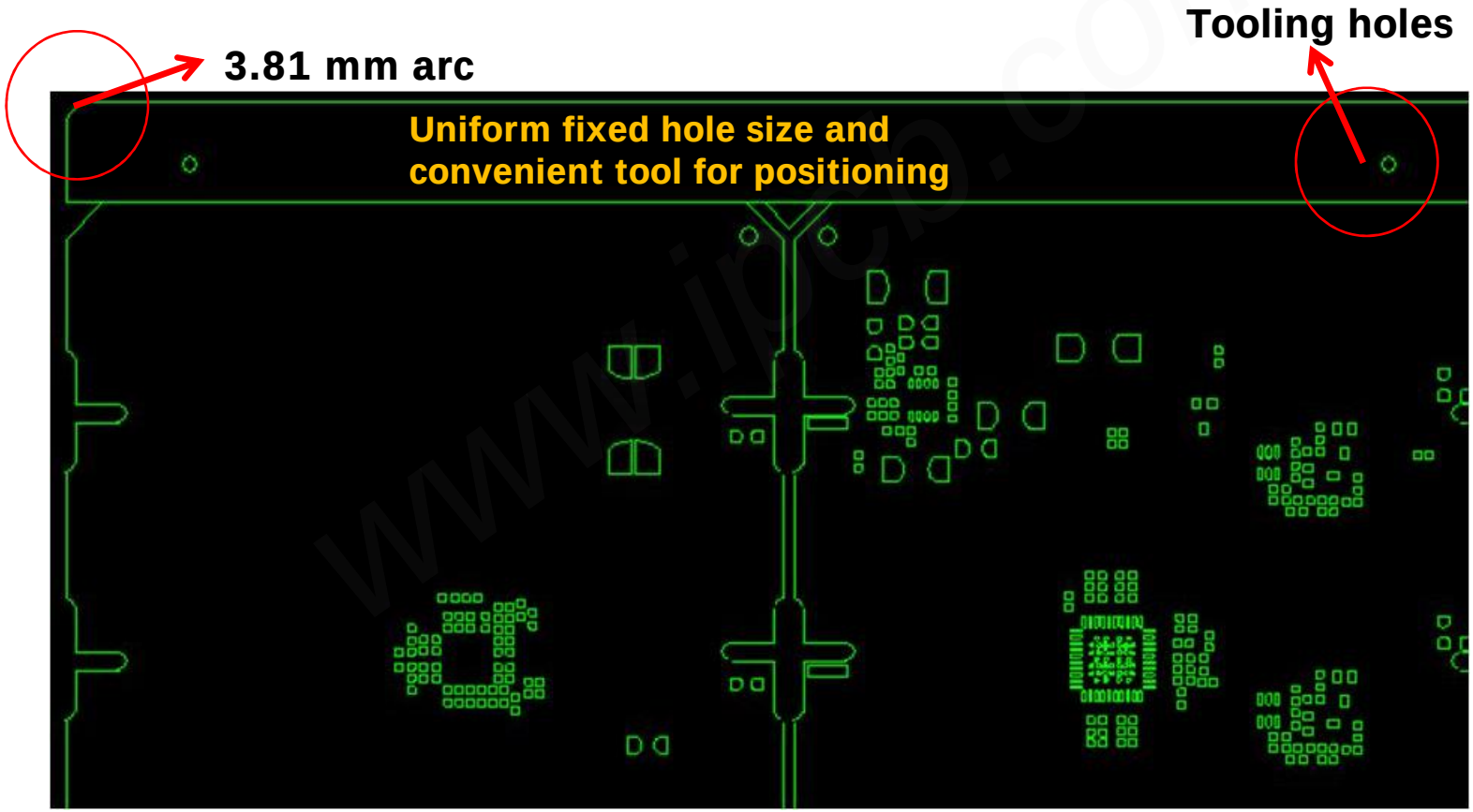


d= 1.0mm
D=3.0mm

- Three fiducial mark-out located diagonally on board, and do follow related dimension requirement . fiducial mark dimension is 1mm(d) and solder mask is 3mm(D) . The diagonal fiducial mark should not be symmetrical, it should be keep away at 5 mm.
- Fiducial PAD edge keep 4mm distance from the edge of PCB
- Single board must have two fiducial mark –in located diagonally on the board.

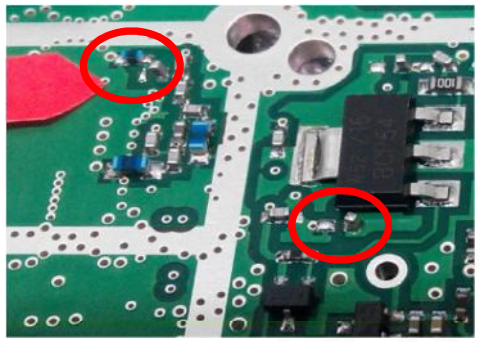
PCB fixed position hole

- Tooling holes on all boards are called out with correct dimensions, tolerances, and are non-plated. (3.55mm +0.075/-0 or 2.18mm +0.05/-0.05)
- There should be 3.81 mm arc located at 4 corners of PCB to avoid stuck at conveyor and damage of packing material.



SMT component PAD design

- NG symptom: 0402 chip tombstone
- For example: D500+ FN700054 chip 0402 chip tombstone defect rate:1.0%
- NG picture:



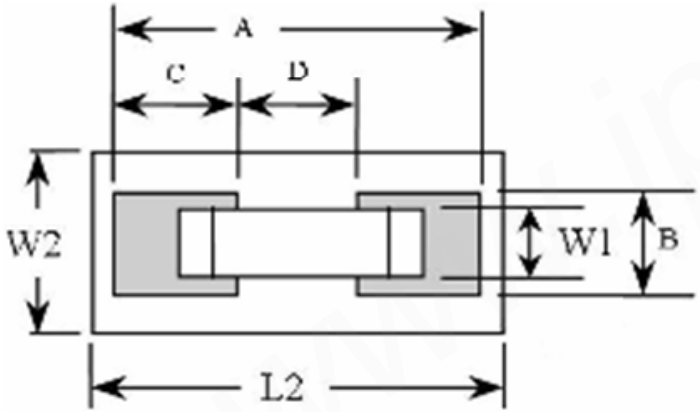
- Analysis: PAD to PAD space is too big caused the tombstone after IR .

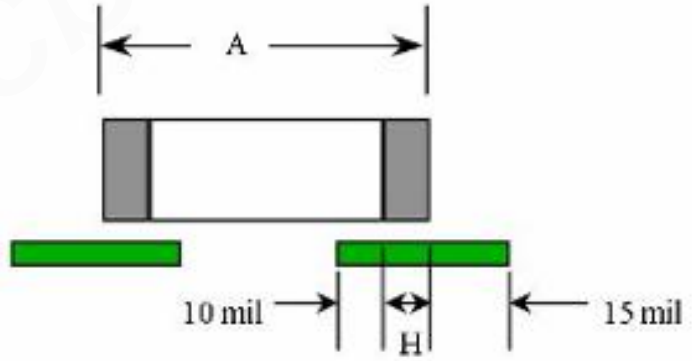
PAD to PAD : 16mil

PAD to PAD : 22mil

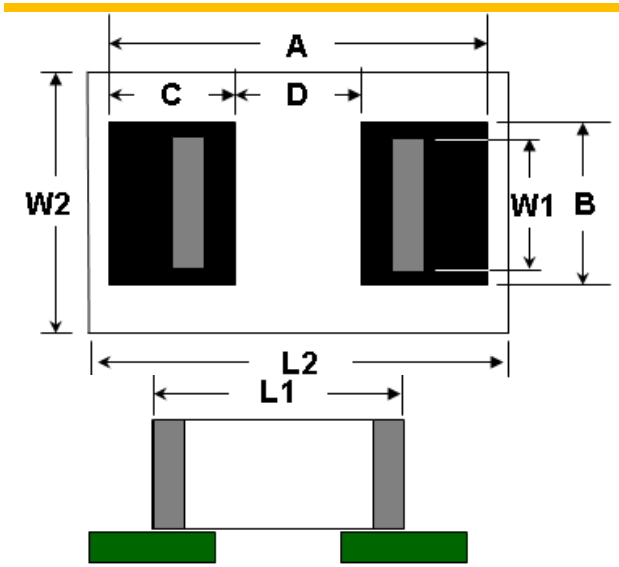
SMT component PAD design

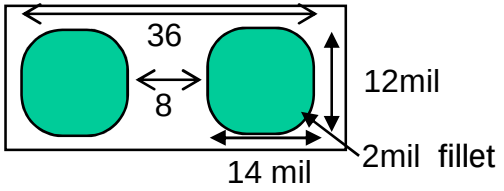
- **Non specifications within RLC Pad design according to the following principles**
  - **(i) B= max of W1, to prevent the shift**
  - **(ii) C=10 + H(electrode width) + 15 mil**
  - **(iv) restricted area L2: A+10mil ,W2=max: (" W1 + 8 + max of tolerance" , " B + 10 ")**



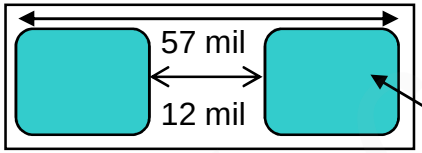


SMT component PAD design





0201 PAD design



0402 PAD design

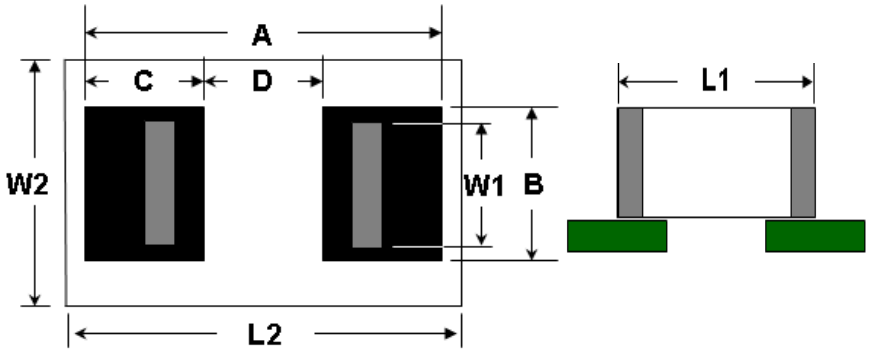
Note: besides the chip 0201/0402,the rest of database is for reference only

(1) Resistance and inductance components size list unit: mil

TYPE	Body Size(mil)		Component body tolerance(mm)	Pad Size(mil)			
	L1	W1		A	B	C	D
0201(0603)	24	12	±0.03	36	12	14	8
0402(1005)	40	20	±0.05	56	22	22	12
0603(1608)	63	32	±0.1	83	40	31	21
0805(2125)	79	50	±0.2	103	61	37	29
1206(3216)	123	63	±0.25	160	73	50	60
1210(3225)	123	101	±0.2	171	110	55	61
2010(5025)	197	99	±0.25	230	110	45	140
2512(6432)	252	126	±0.25	290	138	70	150
ref.	L2=A + 10； W2=max: (" W1 + 8 + max of tolerance " , " B + 10 ")						

SMT component PAD design

(2) capacitance component size list



Note: besides the chip 0201/0402,the rest is for reference only

unit: mil

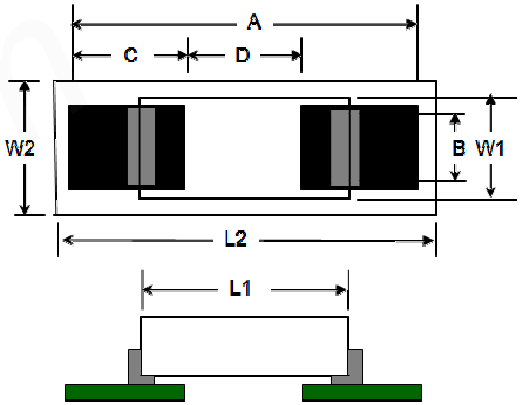
TYPE	Body Size(mil)		Component body tolerance (mm)	Pad Size(min)				Placement Size		area
	L1	W1		A	B	C	D	L2	W2	
0201(0603)	24	12	±0.03	36	12	14	8	51	22	1122
0402(1005)	40	20	±0.05	56	22	22	12	75	34	2550
0402(1005)	40	20	±0.1~0.2	60	28	24	12			
0603(1608)	63	32	±0.2	83	40	31	21	105	46	4830
0805(2125)	79	50	±0.25	103	61	37	29	140	76	10640
1206(3216)	126	63	±0.3	160	73	50	60	182	86	15652
1210(3225)	126	99	±0.3	171	110	55	61	190	130	24700
1808(4520)	189	80	±0.3	210	90	50	110	230	120	27600
1812(4532)	182	126	±0.3	207	136	60	87	237	166	39342
ref.	L2=A + 10； W2=max: (" W1 + 8 + max of tolerance " , " B + 10 ")									

SMT component PAD design

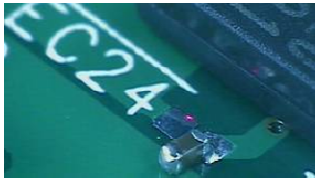
(3) STC3216~7343

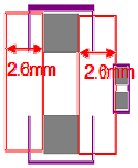
unit: mil

TYPE	Body Size		Pad Size				Placement Size		area
	L1	W1	A	B	C	D	L2	W2	
3216	124	66	176	66	50	76	227	112	25424
3528	142	113	240	90	90	60	283	164	46412
6032	232	130	334	105	90	154	380	180	68400
7343	282	173	338	95	90	158	390	200	78000
ref.	L2=A + 30；W2=component body width+ 20；D=A - 2 x C;								



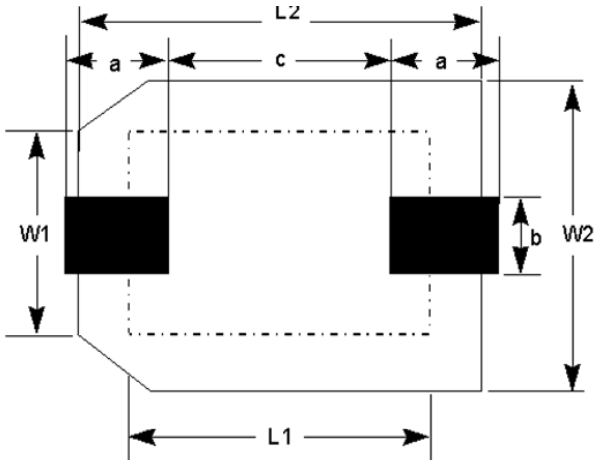
Note : No chips component that size below 0603 located beside 7347 and 6032 tantalum capacitor within 2.6mm pad to pad distance. If un-avoidable, the chip components should be vertical with the tantalum capacitor.





SMT component PAD design

(4)Electrolysis capacitor parts size list



unit:mm

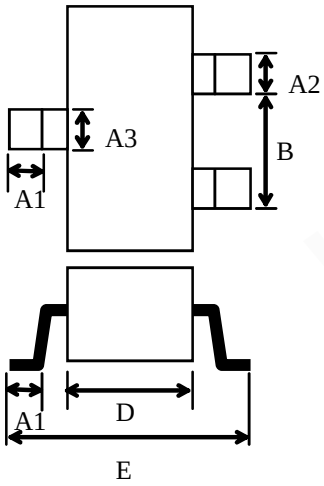
TYPE	Body Size		Pad Size			Placement Size	
	L1	W1	a	b	c	L2	W2
SE3116	8.0	6.3	3.1	1.6	2.2	9.4	7.0
SE2811	6.3	5.0	2.8	1.6	1.4	8.0	5.7
SE2716	6.0	5.0	2.7	1.6	1.4	7.8	5.7
SE2516	5.5	4.0	2.5	1.6	1.0	7.0	4.7

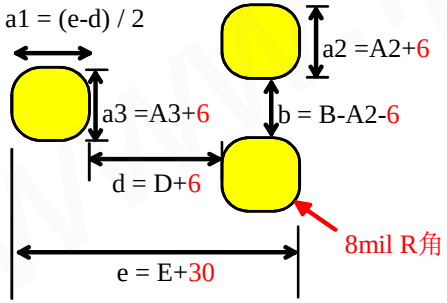
SMT component PAD design

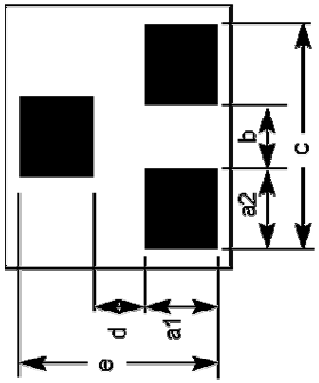
(5)Diode-3PIN

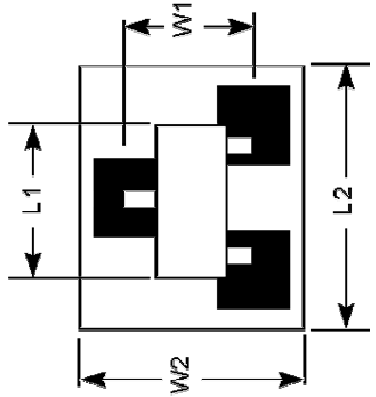
unit: mil

TYPE	Body Size		Pad Size						Placement Size	
	L1	W1	a1	a2	b	c	d	e	L2	W2
SOT-23			48	40	40	120	40	136	136	156
Diode-3PIN			48	40	40	120	40	136	136	156
ref.	W2=e+20 , L2=max(c+16; L1+16)									

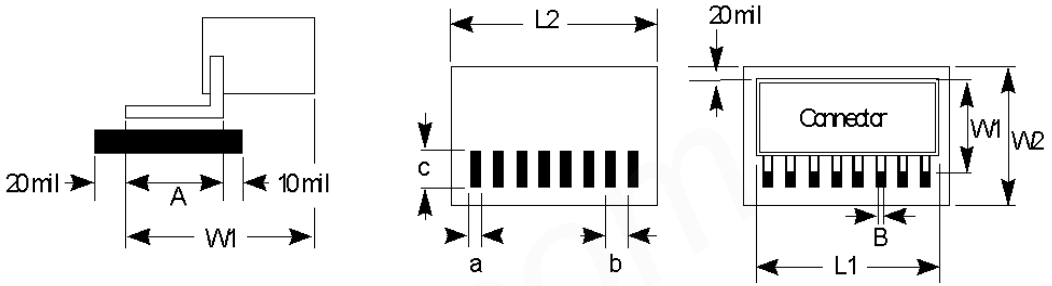








SMT component PAD design



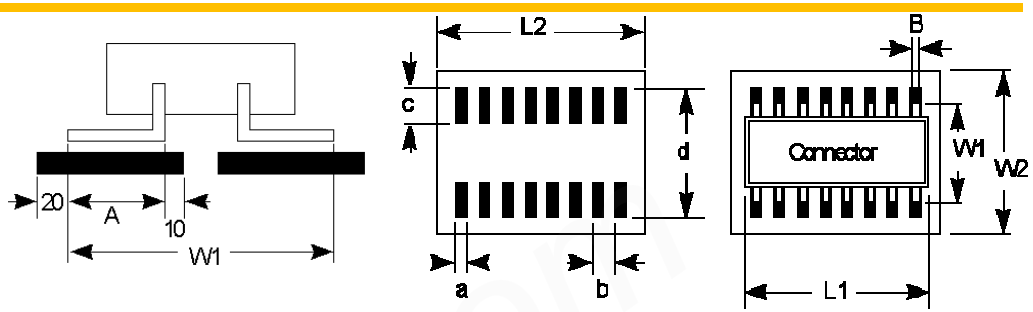
(6) Connector pin for Single side

unit: mil

Pitch, b		Body Size		Pad Size		Placement Size	
(mm)	(mil)	L1	W1	a	c	L2	W2
0.5	19.685			12	A+30	L1+30	W1+50
0.635 0.650	25.00 25.59			14	A+30	L1+30	W1+50
>0.65	>25.59			B+4	A+30	L1+30	W1+50
Note		* If the component pitch be defined by the metric unit , In English units should be considered for the calculation of the cumulative error of Pitch *The distance between connectors should at least have 2mm space from the outline edge of the Pad or Body. *For component higher than 5mm, need to keep same distance/clearance on pcb surface free from component to avoid shadow effect and causing AOI limiation. *The distance between smd type connector and chip should at least have 2mm space from the outline edge of the Pad or Body. *Boss pin hole size (NPTH) = Connector boss size + 0.15 mm					

SMT component PAD design

(7)Connector pin for two side



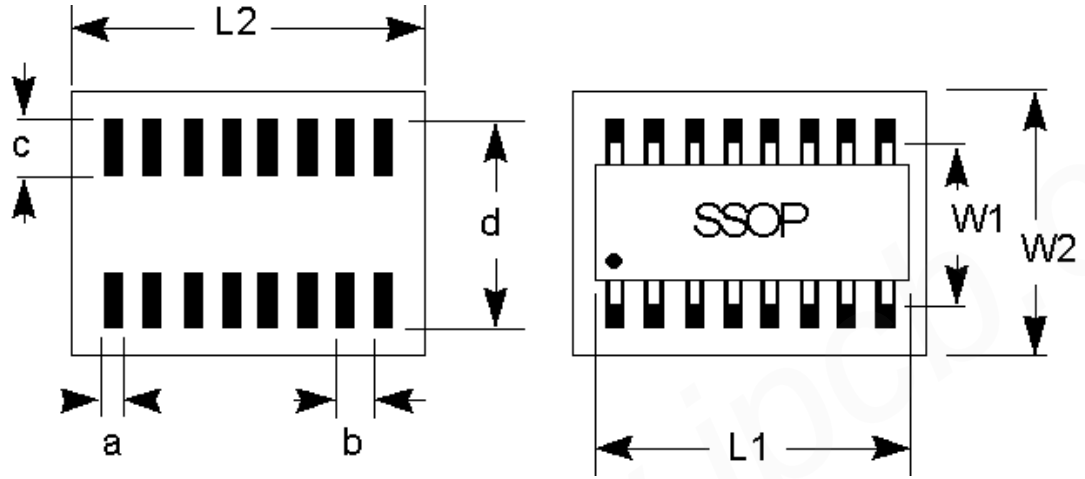
unit: mil

Pitch, b		Body Size		Pad Size			Placement Size	
(mm)	(mil)	L1	W1	a	c	d	L2	W2
0.5	19.685			12	A+30	W1+40	L1+30	d+30
0.635 0.650	25.00 25.59			14	A+30	W1+40	L1+30	d+30
>0.65	>25.59			B+4	A+30	W1+40	L1+30	d+30
Note		* If the component pitch be defined by the metric unit , In English units should be considered for the calculation of the cumulative error of Pitch *The distance between connectors should at least have 2mm space from the outline edge of the Pad or Body. *For component higher than 5mm, need to keep same distance/clearance on pcb surface free from component to avoid shadow effect and causing AOI limiation. *The distance between smd type connector and chip should at least have 2mm space from the outline edge of the Pad or Body.						

SMT component PAD design

(8) IC types

a. SSOP, SOP



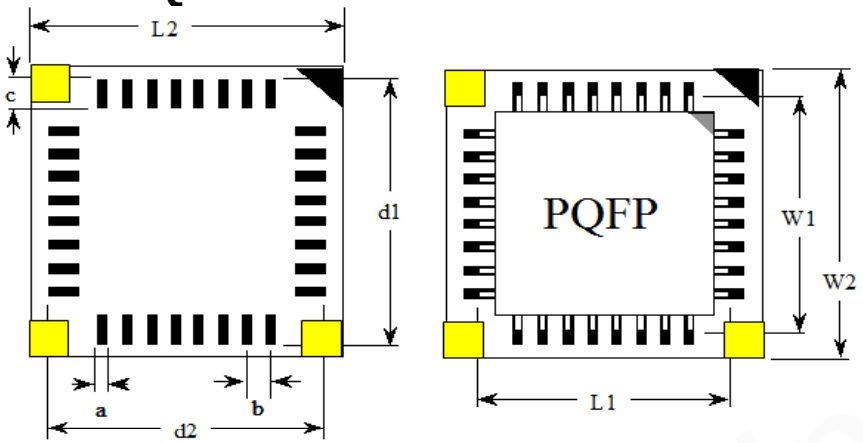
unit: mil

Type	Pitch, b		Body Size		Pad Size			Placement Size	
	(mm)	(mil)	L1	W1	a	c	d	W2	L2
SSOP	0.4	15.748			8	60	W1+30	d+30	L1+20
SSOP	0.5	19.685			12				
SSOP	0.635	25			14				
SSOP	0.65	25.59							
SSOP	0.8	31.496			16				
SOP	1.27	50			25				
	Note		* If the component pitch be defined by the metric unit , In English units should be considered for the calculation of the cumulative error of Pitch						

SMT component PAD design

(8) IC types

b.QFP



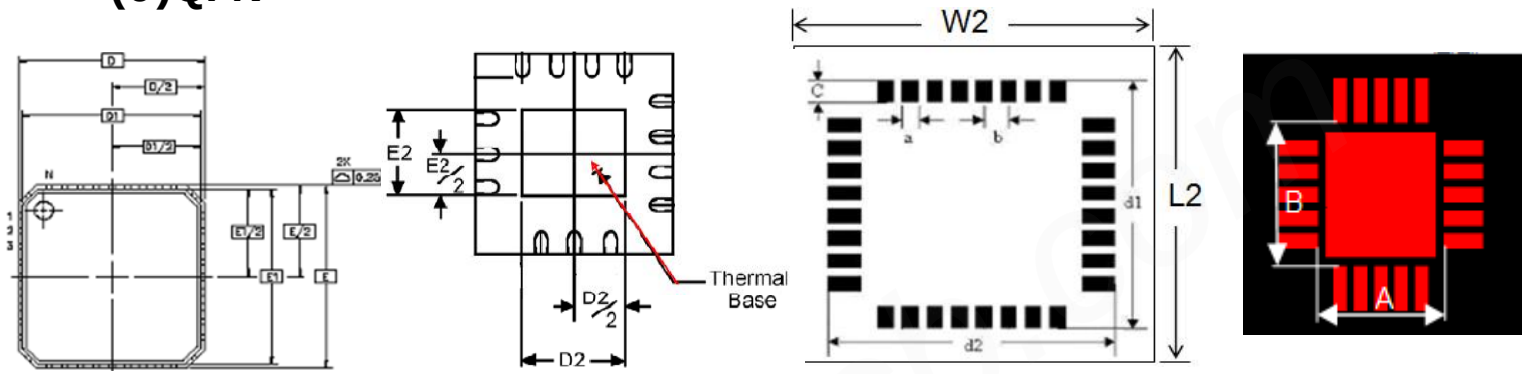
unit: mil

Pitch	Body Size		Pad Size				Placement Size	
b	W1	L1	a	c	d1	d2	W2	L2
19.485 (0.5mm)			12	60	W1+40	L1+40	d1+20	d2+20
25.59 (0.65mm)			16	90	W1+50	L1+50	d1+20	d2+20
31.496 (0.8mm)			18	90	W1+50	L1+50	d1+20	d2+20
Note	•If the component pitch be defined by the metric unit , In English units should be considered for the calculation of the cumulative error of Pitch							

SMT component PAD design

§ **IC types**

(9)QFN

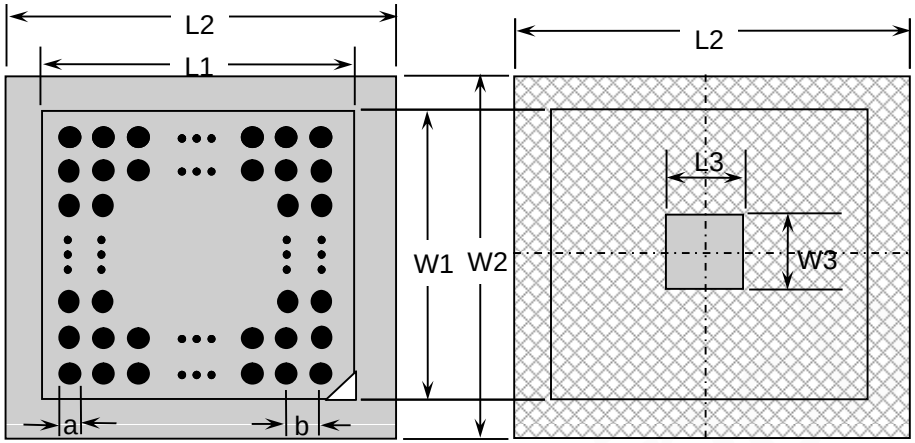


unit: mil

Pitch	Body Size		Pad Size				Placement Size	
b	D	E	a	c	d1	d2	L2	W2
19.485 (0.5mm)			12	60	E+40 (On both sides of the 20)	D+40 (On both sides of the 20)	d1+30	d2+30
25.59 (0.65mm)			14	60	E+40 (On both sides of the 20)	D+40 (On both sides of the 20)	d1+30	d2+30
Note	Ground pad at the bottom of the QFN : A - D2 >= 0.4 mm; B - E2 >= 0.4 mm							

SMT component PAD design

– **BGA, CSP**



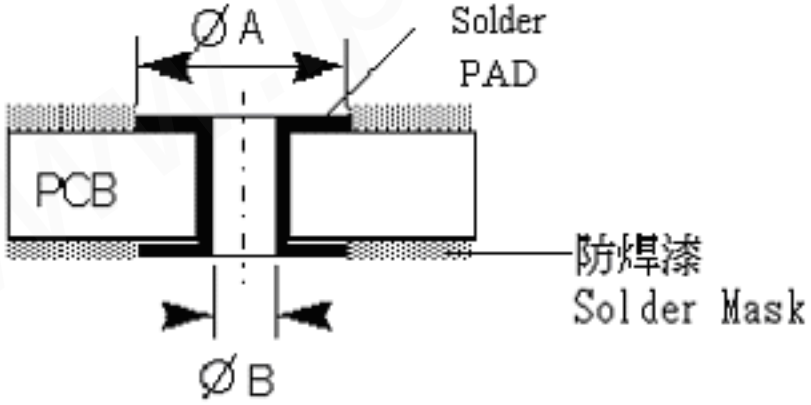
unit: mil

Pitch ,b		Body Size		Pad Size	Placement Size	
(mm)	(mil)	L1	W1	a	L2	W2
CSP		<= 5 mm	<= 5mm		L1+80	W1+80
BGA		> 5mm	> 5mm		L1+120	W1+120
Note		*Don't overlap with any component. *Don't put the range of Connector, BGA and other large easy to heat parts. All of the Via Hole shall be double coverage of solder mask layers				

PTH component PAD design

- **In order to simplify and improve the printing circuit welding (soldering) process , The special development of through-hole reflow technology (Pin-in-Paste) The through-hole type connector from Dipping process ,change to SMT printing solder paste and reflow replaced .** Place all thru-hole parts on topside of the board. (Avoid manual soldering process)

- **B : aperture size≧pin diameter size +0.25 mm (10 mil)**
- **A : The outer layer of the minimum pad size ≧ aperture size+ 0.36 mm (14 mil)**
- **According to th) = Hole size (ΦB) + 40 mil**



【剖視圖】Side View

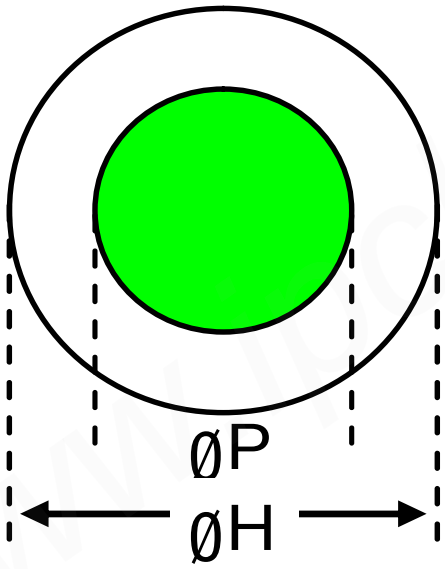
PTH component PAD design

PTH design guideline

Parts of pin diameter and through the aperture ratio (PH) principle:

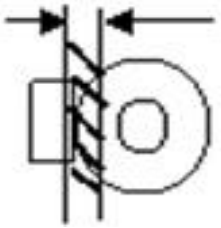
Pin to hole rate (ØP / ØH) should fall within 0.6~0.8, shown as diagram:

PH= 0.6~0.8 the best ; PH= 0.4~0.5 Acceptable ; PH < 0.3 not acceptable

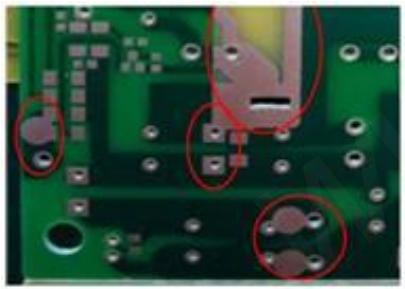


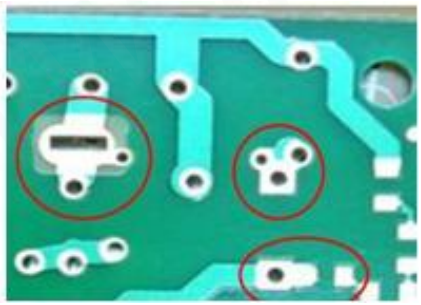
PTH component PAD design

- If any annular ring of PTH connect with connector or PTH pad, please add solder mask to isolate each other (width



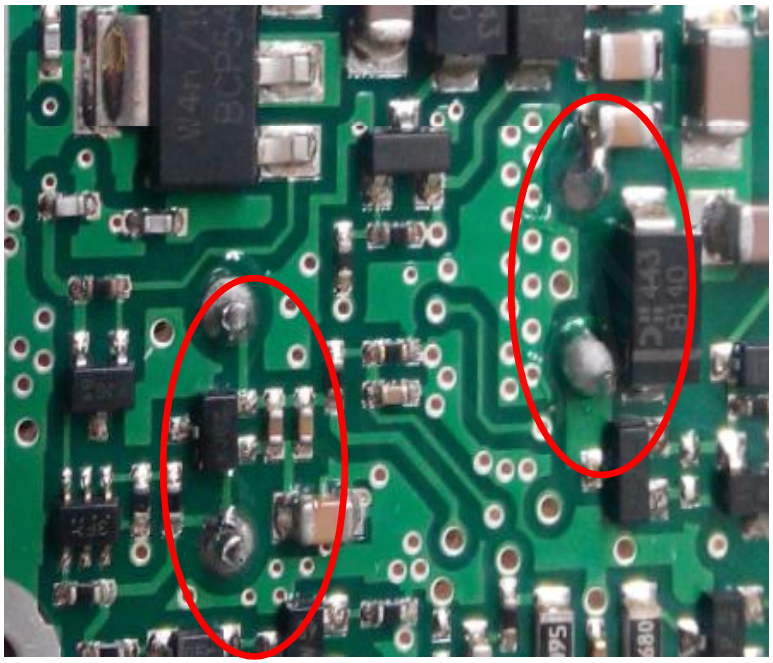
As PSU A000116 Design issue, between PAD with Ground no solder mask covered cause the solder bridge /empty solder.





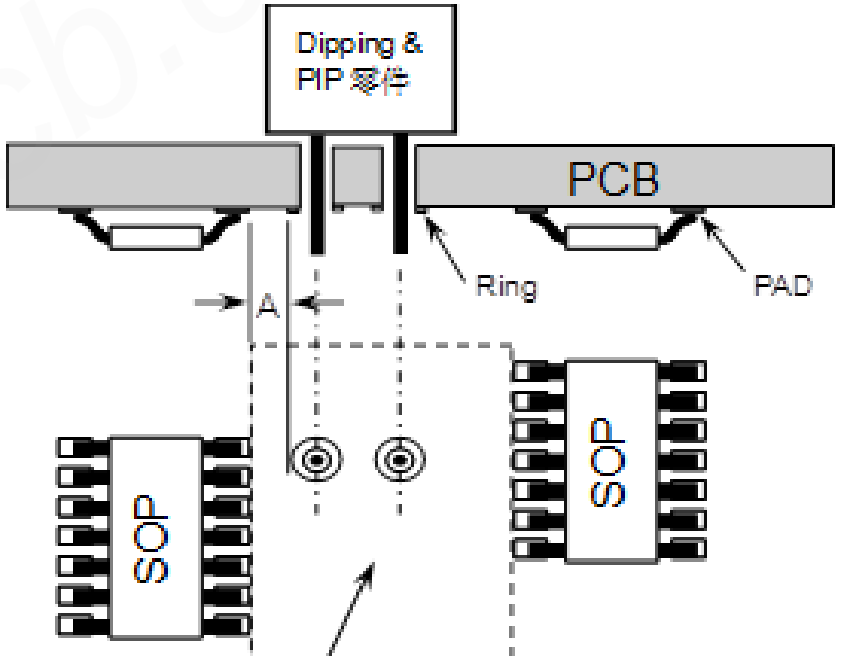
PTH component PAD design

- The distance between the PTH and chips too is very close when manual solder has the risk for broken and solder short . besides arrange Ops to manual solder ,no choice, Waste a lot of manpower and delay output



PTH restricted zone:

- For pin in paste process, keep at least 3mm distance between edge of hole ring and pad.



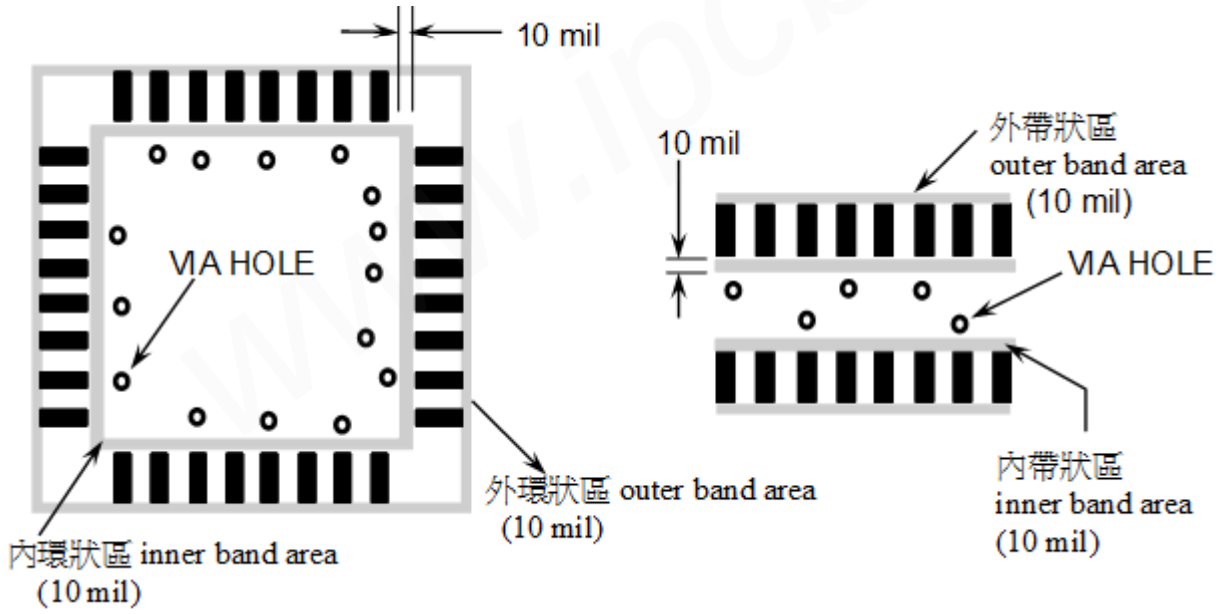
Through-hole(Via)design

Via hole under the component body

Via hole under the smt component body ,need to confirm this PCB **whether through wave soldering process ,**if so, need to blind and buried via hole. **Otherwise, there will be the risk of overflow from the hole of Via solder.**

(1) The normal PAD layout (Within the PAD pins)

- Inner band area (10mil) Via Hole can not be placed.
- outline band area(10mil) ,Via Hole can not be placed.

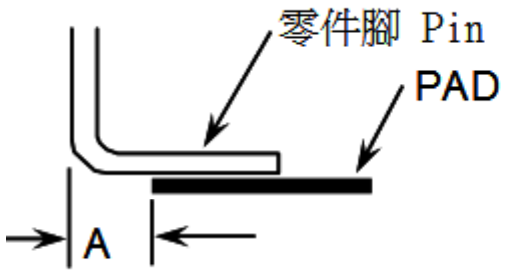


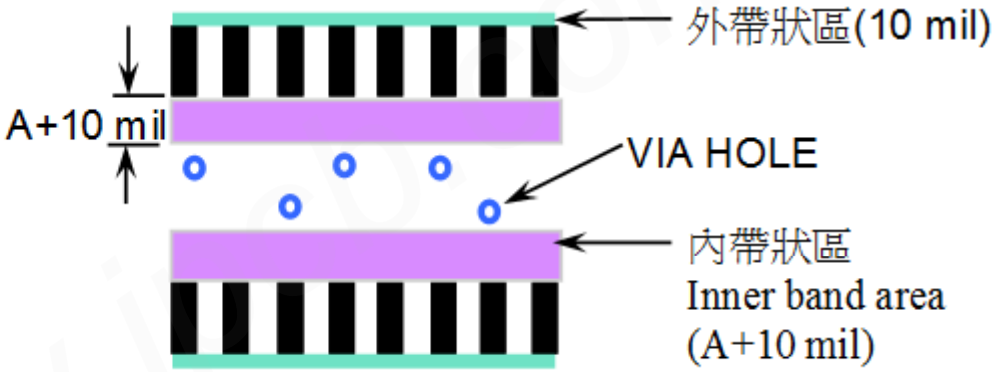
Through-hole(Via)design

Via hole under the component body

(2) Un-normal PAD layout (the pin of the component over the PAD)

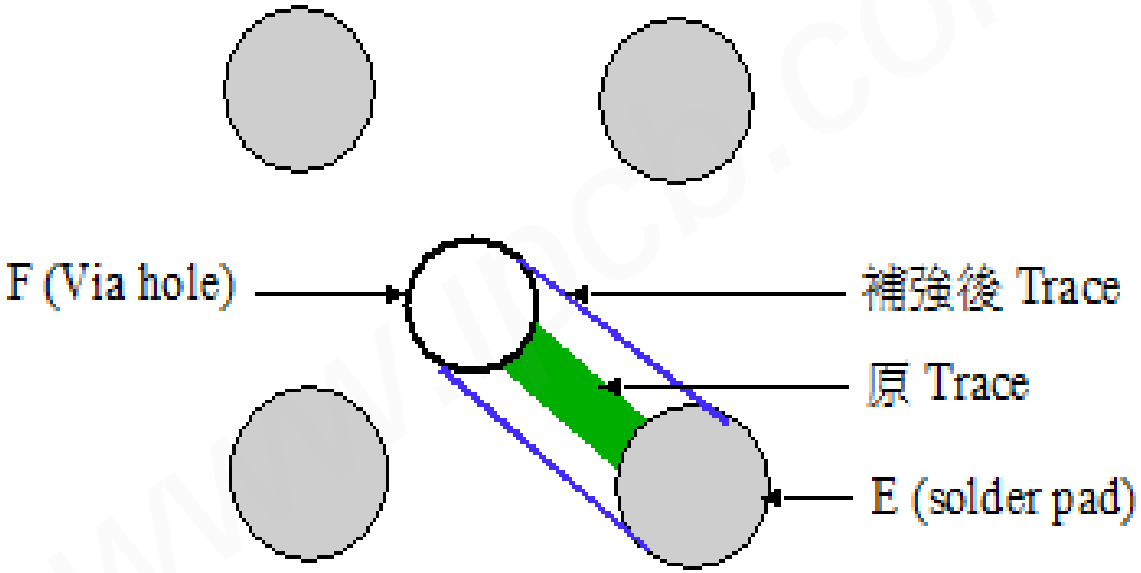
- inner band area (A + 10mil) Via Hole can not be placed
- outline band area (10mil) Via Hole can not be placed





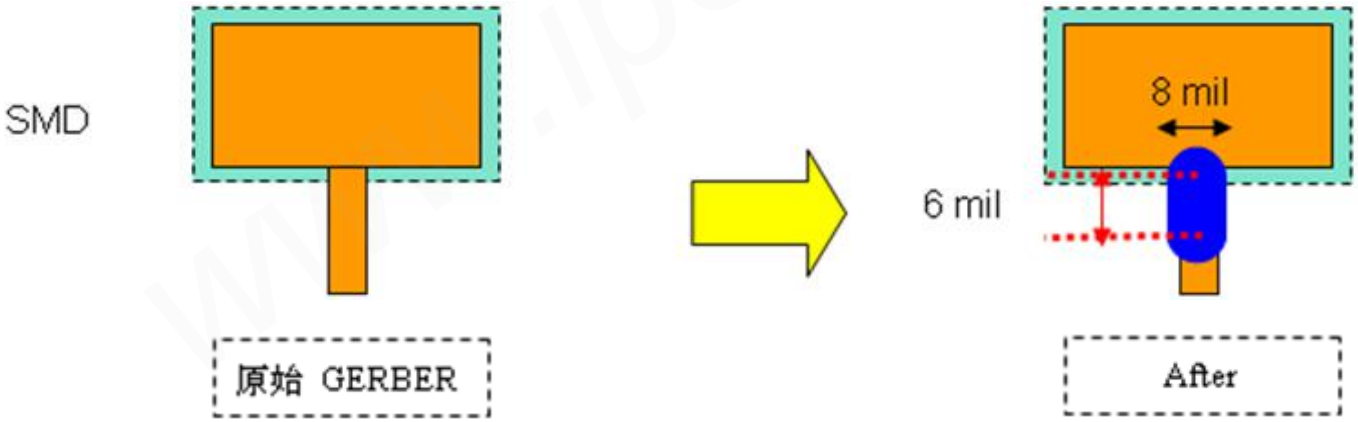
Trace design

- Power Trace to strengthen
  - PAD/Via hole with Trace to junction need to strengthen，the general way (Power Trace，the rest of type refer to Tear drop design)



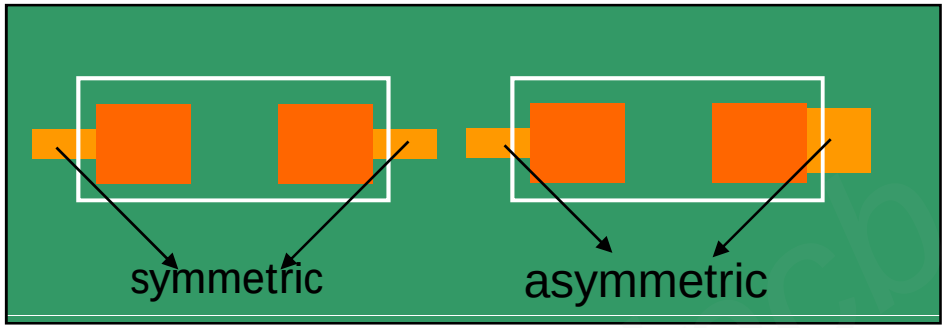
Trace design

- Add tear drop
  - In the outer trace add tear drop as below icon:
  - (1) When the line width is less than 8 mil ,In pad and trace junction with width of 8 mil and length of 6 mil trace .
  - (2) When the line width is more than 8min,do not add Tear Drop
  - (3) If the distance is not enough to add a Tear Drop, can be ignored.

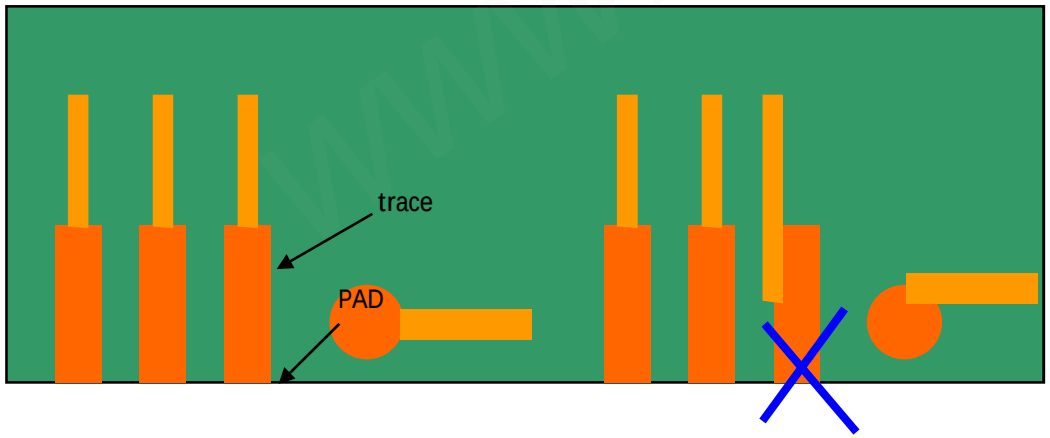


Trace lead the way

Keep symmetric trace design

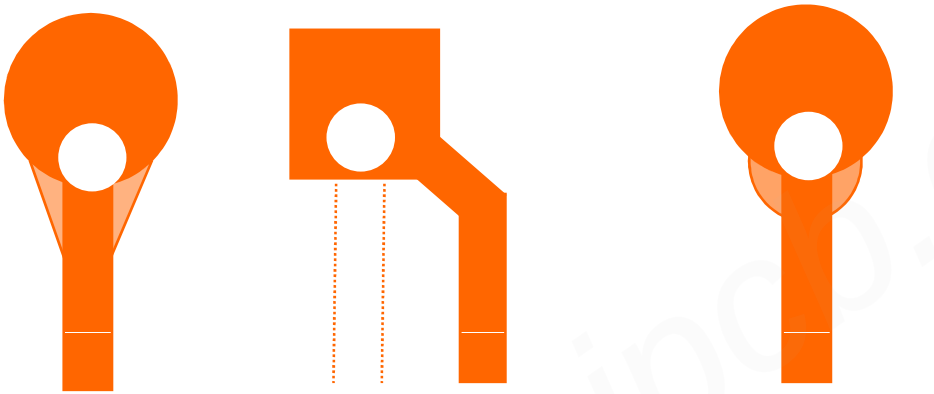


Trace from the center of the pad



Trace design

- Trace line and the hole,be recommended in the following.



•Filleting

•Corner Entry

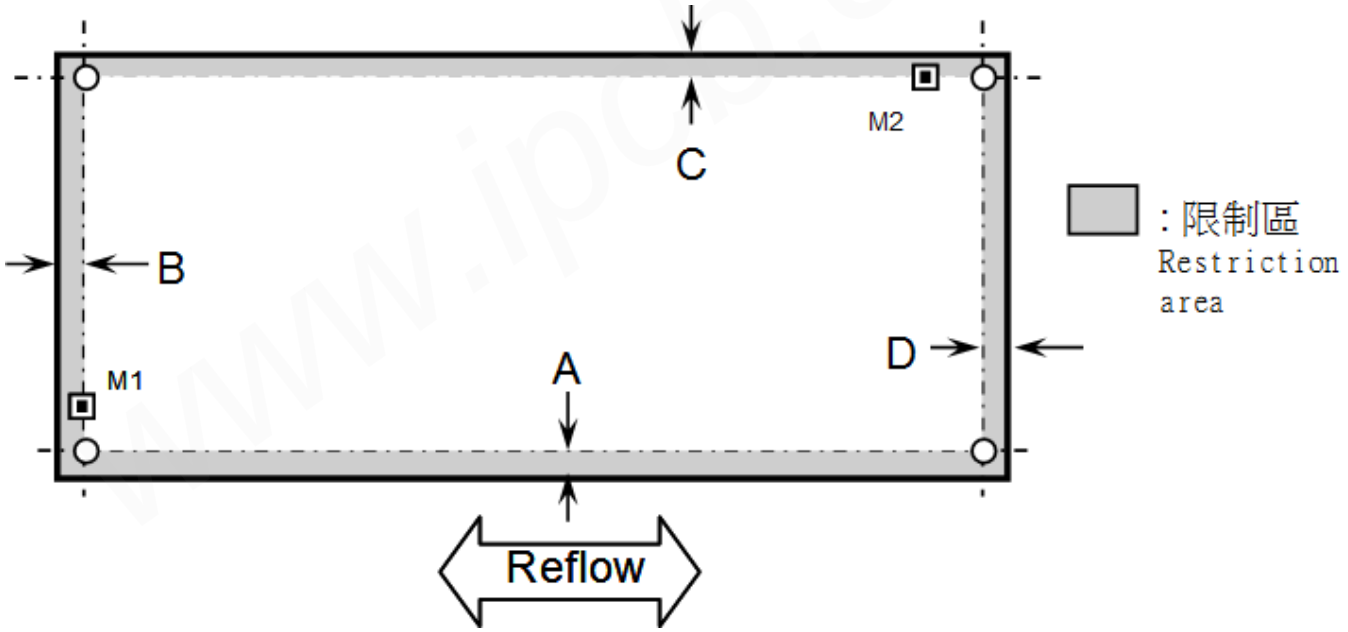
•Key Holing

Other limitation

Component placement limitation

Board edge parts restriction (including the process edge size)

(i) In SMT stage, there should be no any component body or pad within 4 mm along pcb edge that used for conveyor transfer.(as below the upper and the lower sides), Within 2 mm from pcb edge that vertical to the conveyor. PIP or PTH component body should not out of pcb edge.

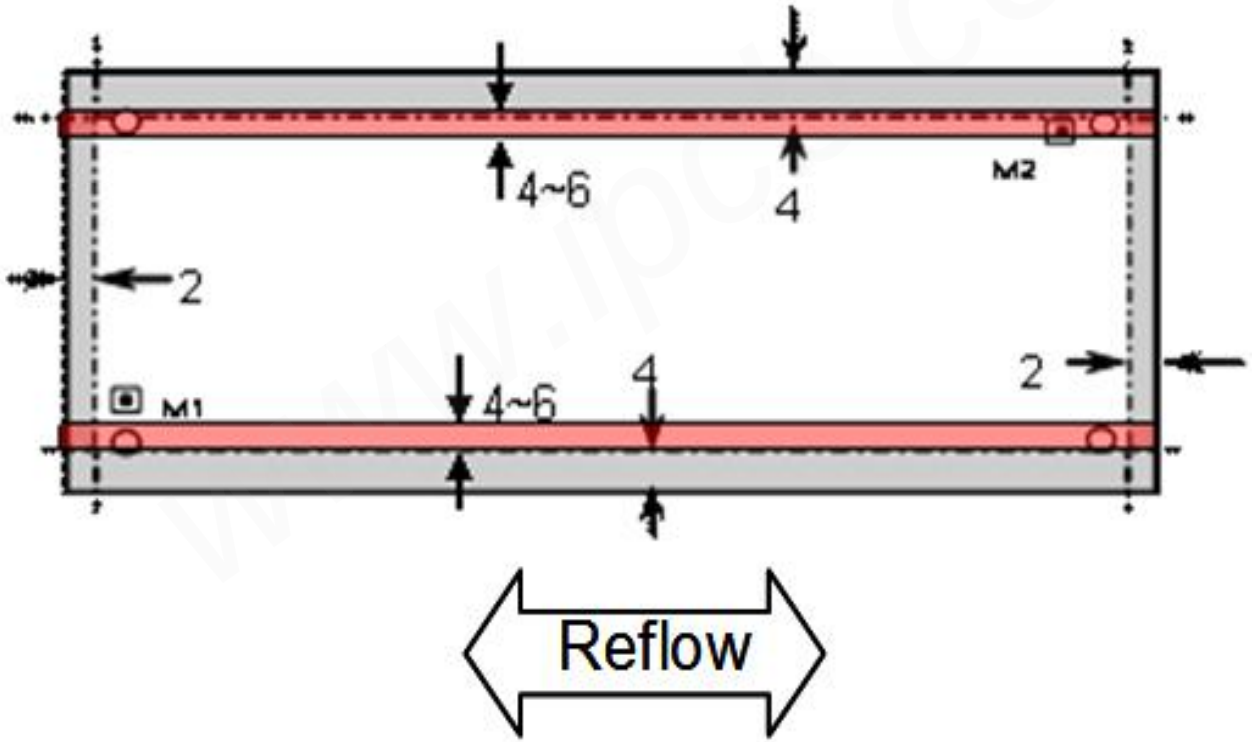


Other limitation

Component placement limitation

Board edge parts restriction (including the process edge size)

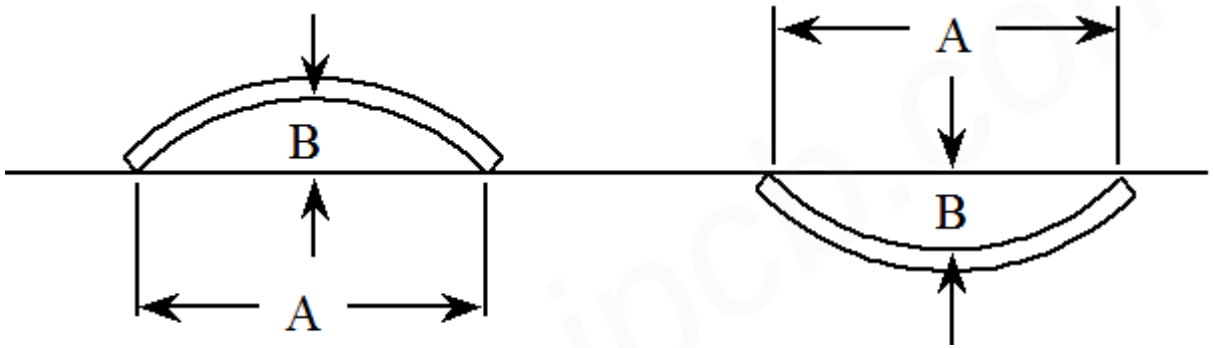
– (ii) In SMT stage, the component height should lower than 2 mm when it away from pcb edge 4~6mm (indicated in pink color region).



Other limitation

Deformation limit

- **B/A≤7.5/1000, and the maximum deformation of B must be less than 1.2 mm**
- **PCB thickness limit: 1 ~ 1.6 ± 0.127 mm or 10%**



PCB substance selection

- **The pcb prepreg should meet criteria of Tg ≧145℃.**
- **The pcb prepreg should meet criteria of Td>320 ℃.**

Other limitation

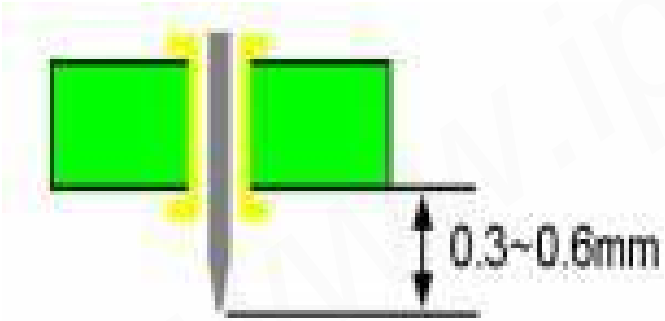
PIP parts limit

- **All of the through hole part must be designed in second to avoid the use of hand soldering process The first surface is necessary to use the SMD TYPE part or through hole parts pin and parts body can not outstand PCB second surface**

- **The spec of pin out of pcb surface in PIP process :**

  pin length ≒ PCB thickness + 0.3~0.6 mm

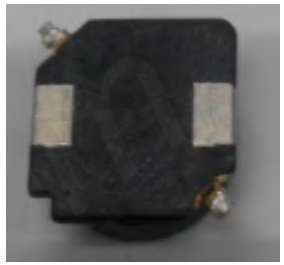
  The insert parts in PCB can not tilt, dumping or easy to loose state.



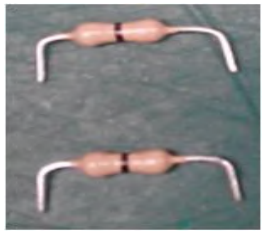
Other limitation

Choose the component :The use of chip components in the SMT stage as far as possible, reduce the waste of human action.

PTH parts to SMD

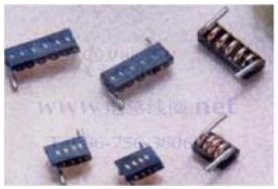


PTH parts to SMD



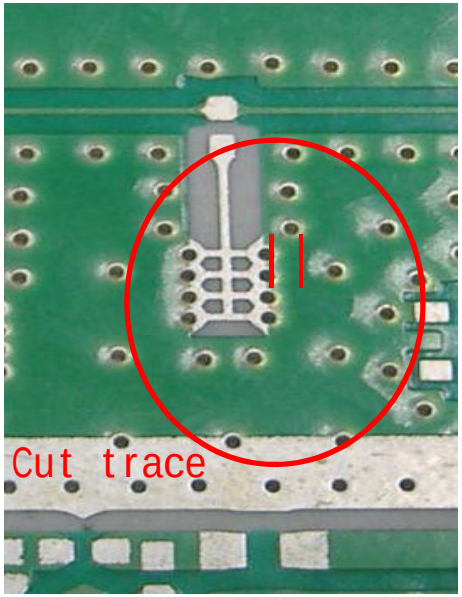
PTH parts to SMD

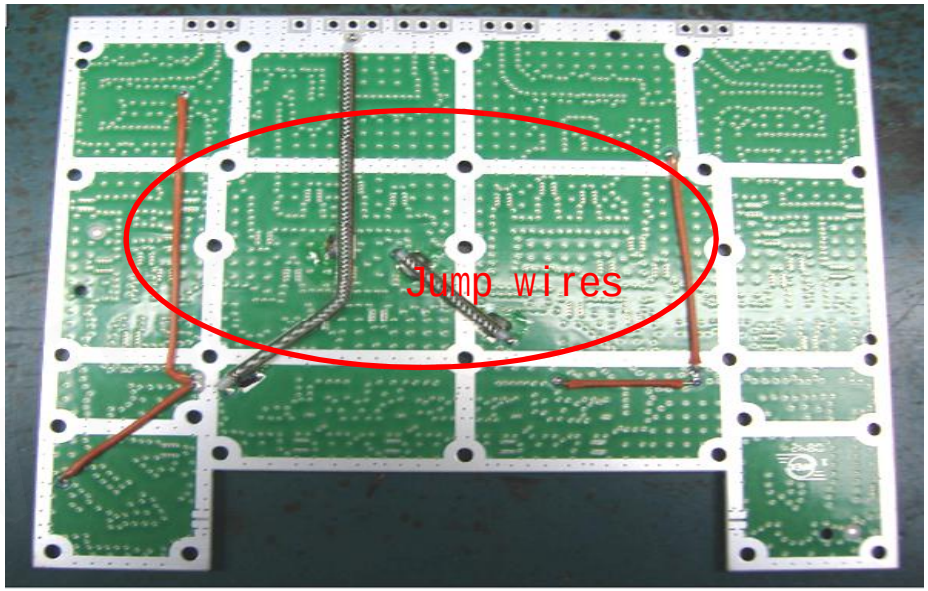
PTH parts to SMD



Other limitation

- **No trace cutting or jump wires process on mass production models.**

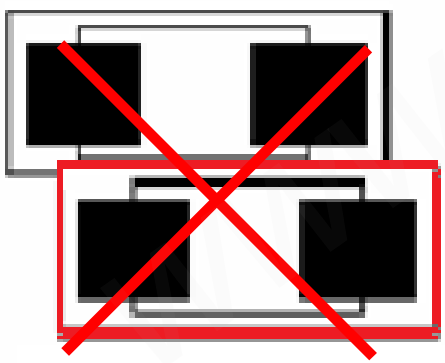




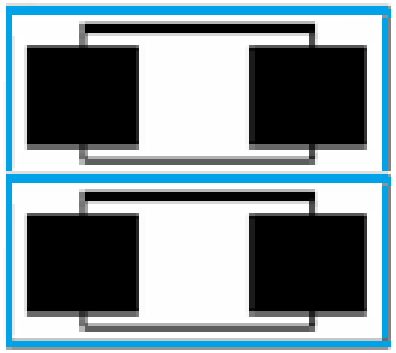
Other limitation

- **PCB pad size should be match with the size of components , If the same parts have different appearance size ,the Layout or according to process proposals to special Layout, must conform the rule。All of pad design need to non-solder mask design.**

  - **Passive component pad size**
  - **The general RLC component： place outline area do not overlap**



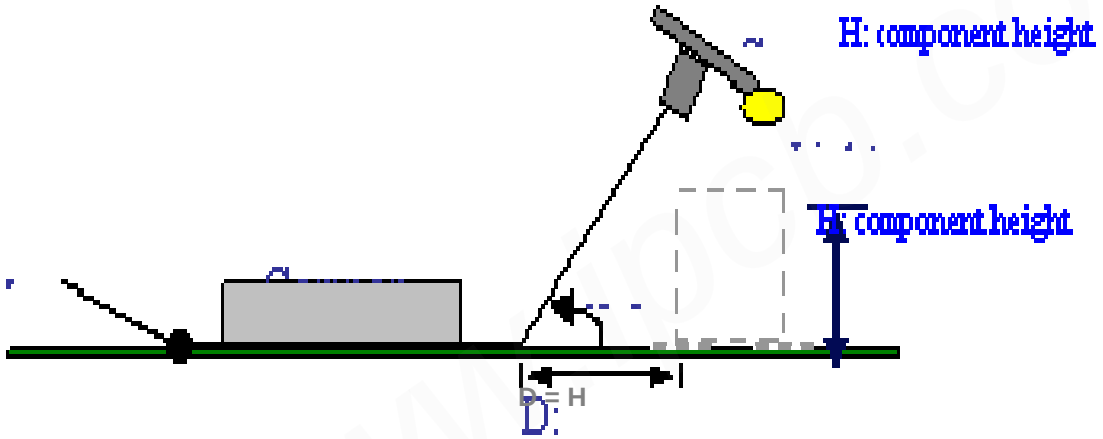
置放區域重疊



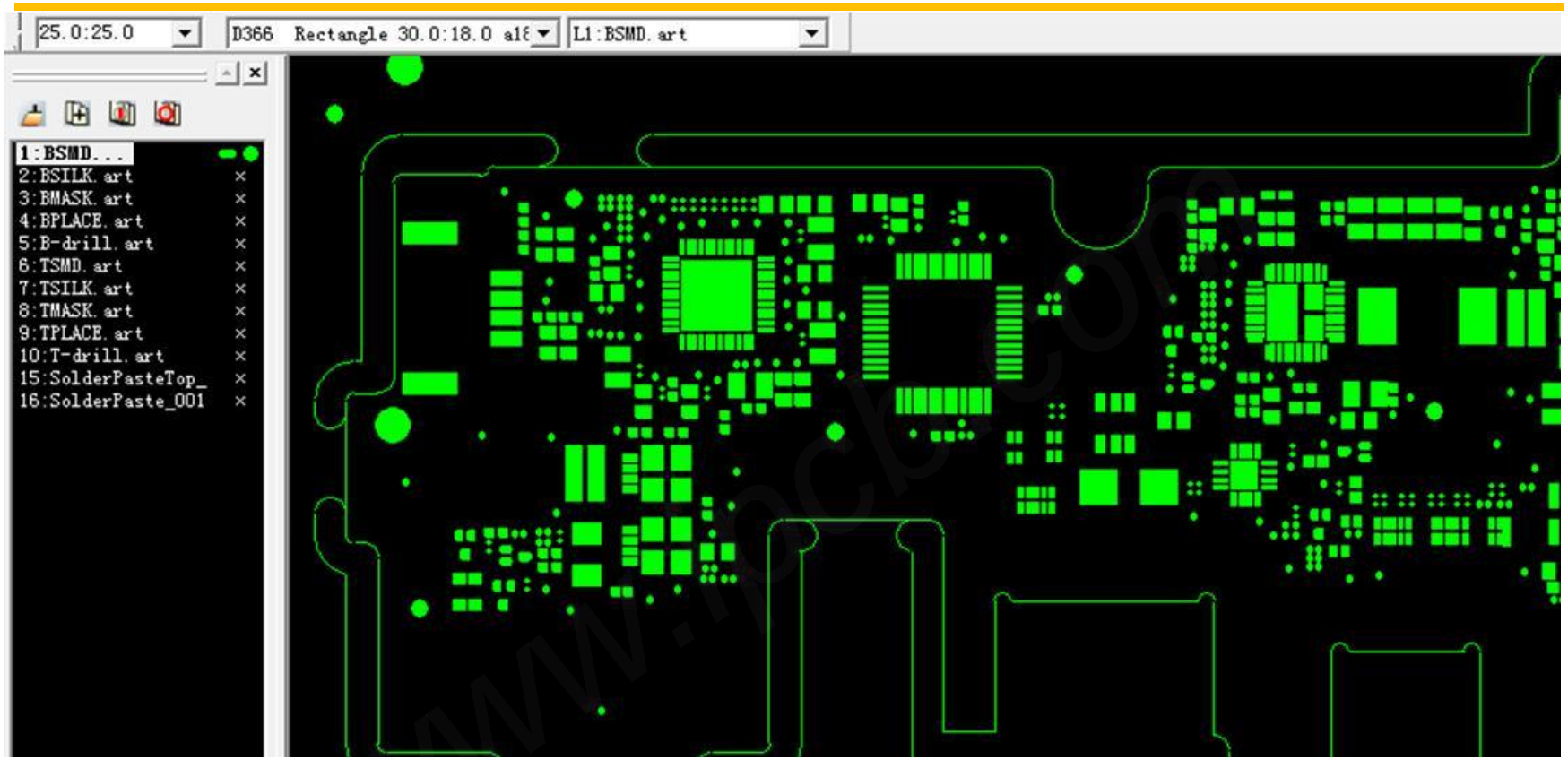
置放區域不重疊

Other limitation

- **For component higher than 5mm, need to keep same distance/clearance on pcb surface free from component to avoid shadow effect and causing AOI limiation.**

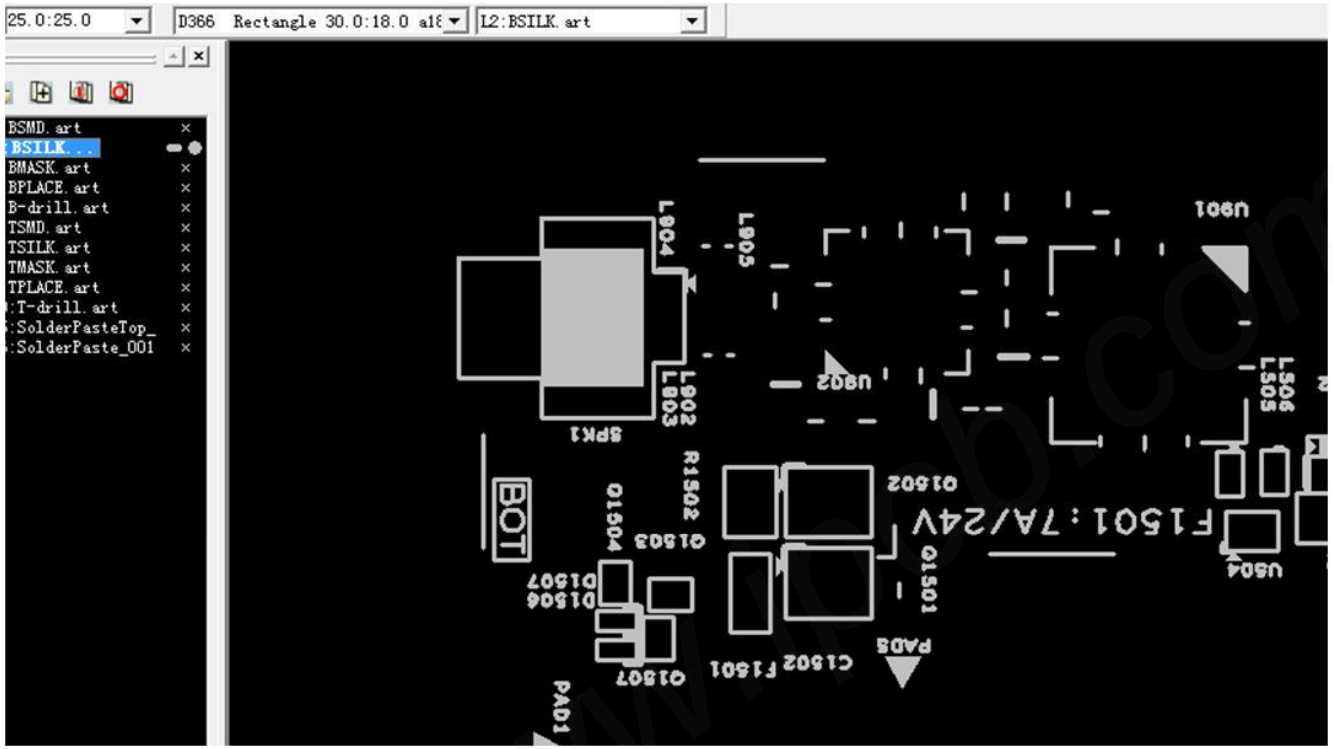


Gerber file layers requirement

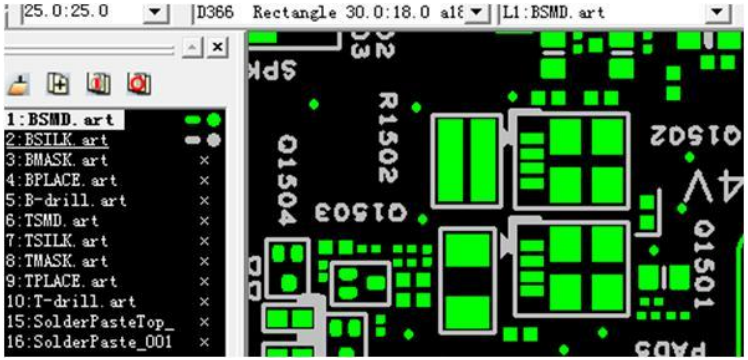


SMD layer: component PAD , reference this layer to design stencil aperture

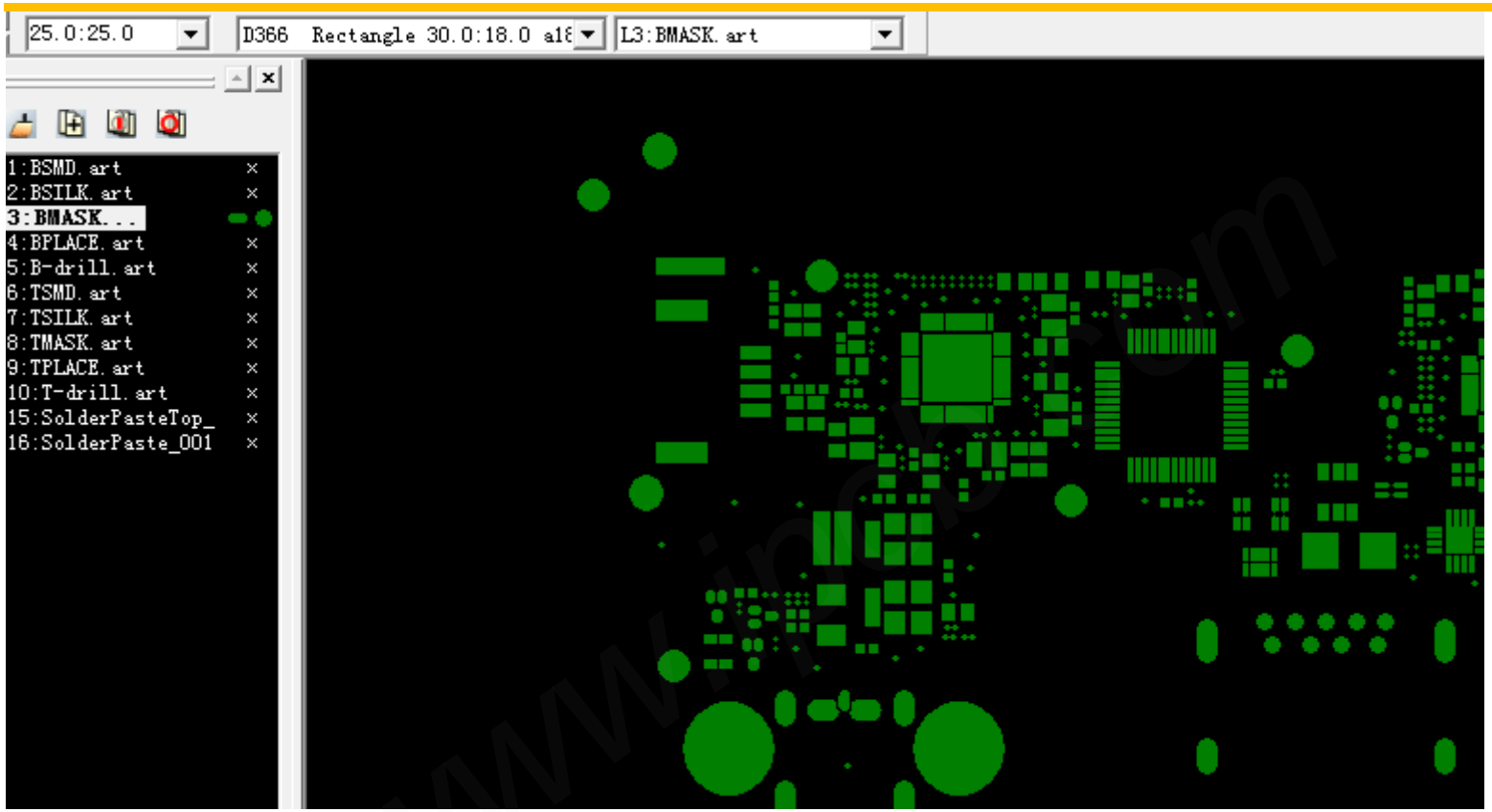
Gerber file layers requirement



Silk layer: SMD component text marking include body outline , pin assignment ,component name ,polarity marking

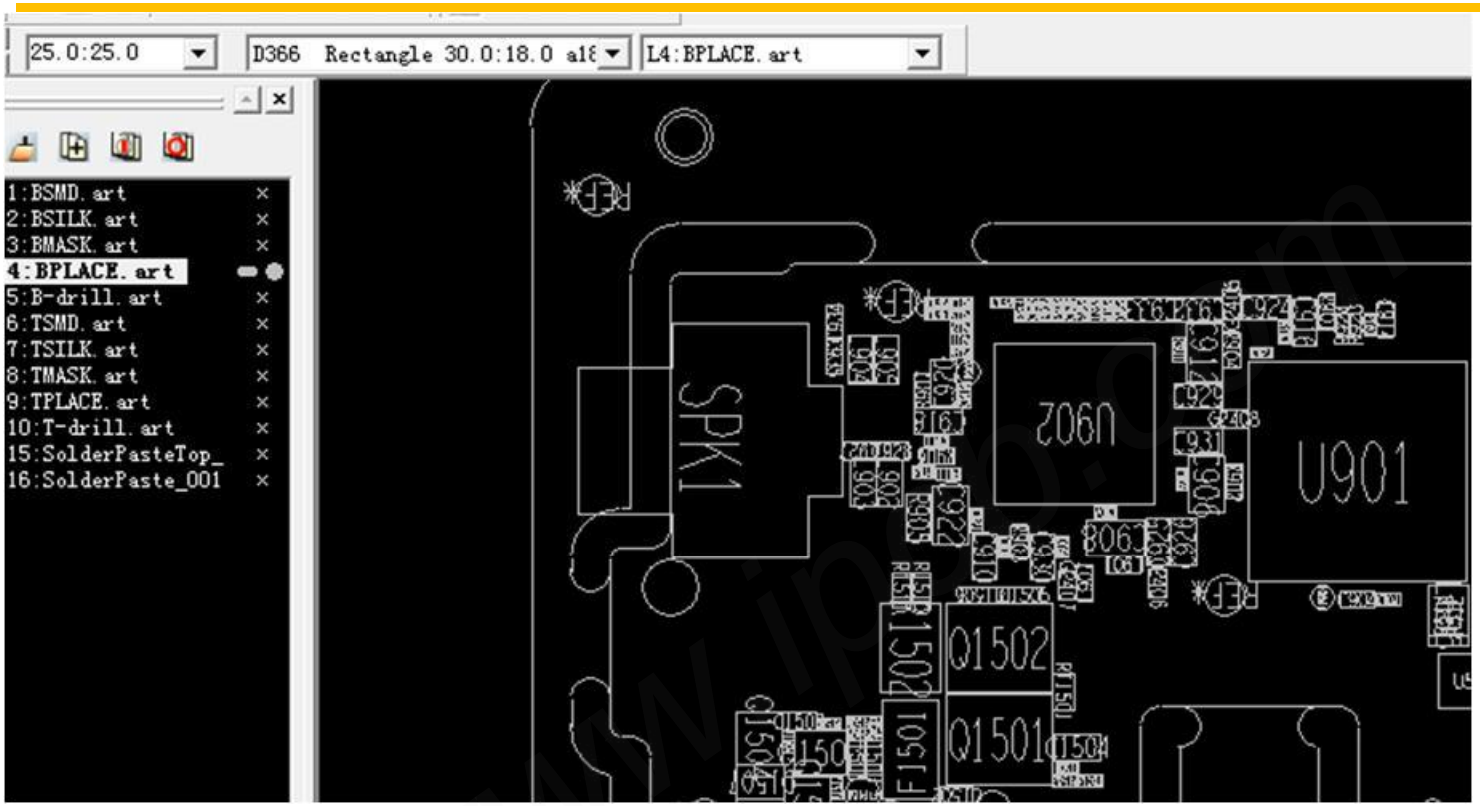


Gerber file layers requirement



Solder mask layer

Gerber file layers requirement



Place layer :check the component location

Gerber file layers requirement

Drill layer :confirm the through-hole size whether it match with the component

Thank You !